DFM & DFA : Building Your Space-Grade PCB Right-First-Time

You have just completed the layout of your latest space-electronics' project, simulated and verified the physical implementations of your circuits, and are now ready to email the stack details as well as ODB++ or RS-274X Gerber files to your fabricator. The customer wants their tested hardware next month and you have budget for a single spin. Does this sound familiar? To ensure your board is built right-first-time, there are Design-for-Manufacturing (DFM) checks to ensure the artwork complies with formal standards and what the fabricator can make, *e.g.* minimum trace width, conductor spacing, via aspect ratio or the smallest clearance between a pad and a nearby track that if violated, could result in bridging during imaging, etching, plating or soldering, creating a short-circuit.

When a PCB fabricator receives your layout files, they typically make a series of DFM checks to ensure the artwork can be tooled to fabricate a reliable and functioning board. Your layout software will allow you to specify which layers to connect, but it may not stop you making choices that cannot be manufactured. Your PCB should be designed in a way to guarantee it can be built and DFM should confirm its manufacturability.

To ensure your PCB is fabricated right-first-time, DFM and DFA require investment in time and effort. Given today's time-to-orbit needs, this can be a challenge for many OEMs, however, Figure 1 illustrates the cost and impact of having to re-spin a PCB after discovering the first one has not been manufactured correctly or the initial product build is faulty. Time is money! The DFM process typically involves discussions back and forth between the customer and the fabricator, depending on the quality requirements and complexity of the design. If the layout engineer understands the fabrication processes and how their design is brought to life, this will increase reliability and yield at the same time as reducing cost and lead-time. This strategy must be planned, occur as the stack is being designed and before routing takes place to ensure a right-first-time board is manufactured to cost and schedule. Your design will deliver the expected performance and you will have better control over the build. Ensuring manufacturability can change the way you envisaged your PCB, *e.g.* it can affect the look, feel, precision and function of your product!

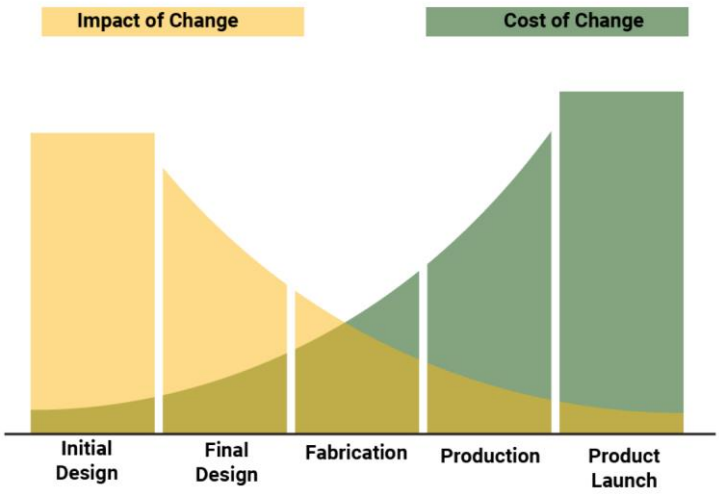

Figure 1 : Impact of PCB re-design and the cost of change.

In this post, I will summarise the DFM checks that should be carried-out before committing to a build, how a multi-layer, HDI PCB is manufactured and the formal standards that need to be followed for space-grade fabrication and assembly.

DFM checks traces, vias, planes, clearances, drilling, solder mask and silkscreen for manufacturing violations, *e.g.* minimum track width, conductor spacing, aspect ratio, distance between a pad and neighbouring copper, smallest hole size and separation, the potential to create acid traps and slivers.

Figure 2 illustrates some of the above DFM checks.

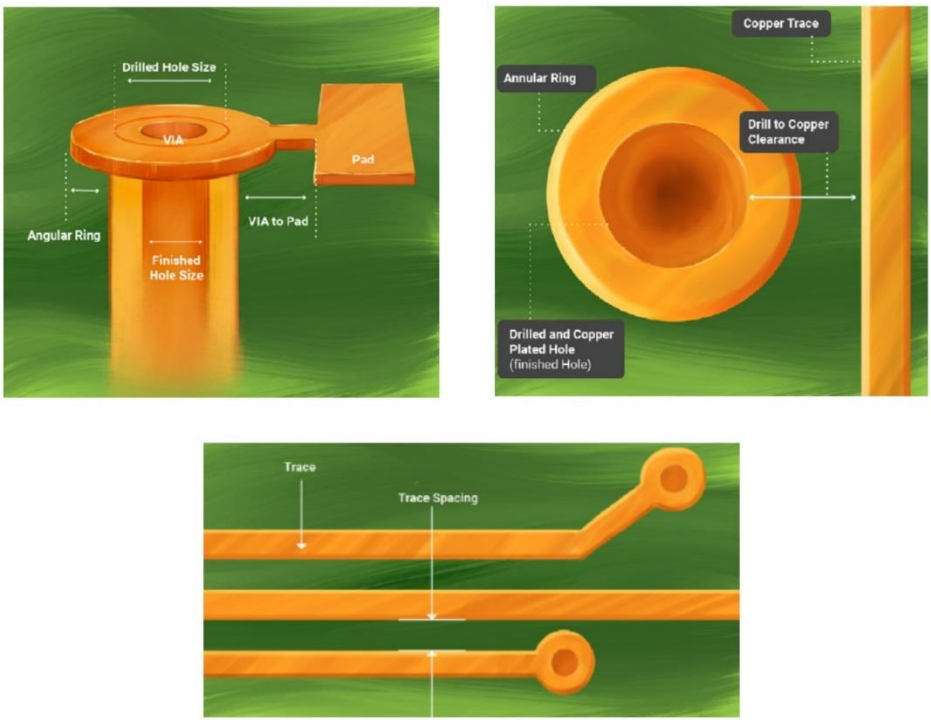

Figure 2 : Illustrations of PCB DFM checks.

The manufacturability of a multi-layer PCB depends on the type, span and quantity of vias, and crucially, the total number of lamination cycles. For non-HDI boards, a single lamination bonds all the layers. HDI designs are built from the centre, initially fusing the inner core and prepreg layers, followed by sequential lamination to add the top and bottom outer layers as well as micro-vias. For reliability reasons, the choice of vias must ensure less than four overall sequential press, drill and plate steps.

The IPC defines different stack-up types and via models for HDI boards: the simplest option is the 0-N-0 stack, where *N* represents the number of layers in the first or core lamination, and 0 denotes no sequential lamination steps, *i.e.* no further dielectric or copper layers are required. The final processing stage is the plating of the through-holes and lasered micro-vias. While this is the lowest cost HDI fabrication, yields and reliability are impacted if the number of layers is too high and long via stubs can create impedance mismatches resulting in reflections.

The 1-N-1 stack adds one sequential lamination either side of the core adding two further copper layers to the top and bottom as illustrated below. The central buried via is mechanically drilled and gets naturally filled with the dielectric material, while the smaller micro-vias are laser drilled. For the same number of overall layers, 1-N-1 has shorter via stubs and smaller aspect ratios than the 0-N-0 standard lamination.

The 2-N-2 stack adds a second sequential lamination adding two further copper layers to the top and bottom, as well as the option of staggered vias as illustrated below. The smaller micro-vias open-up routing channels for HDI BGAs/CGAs.

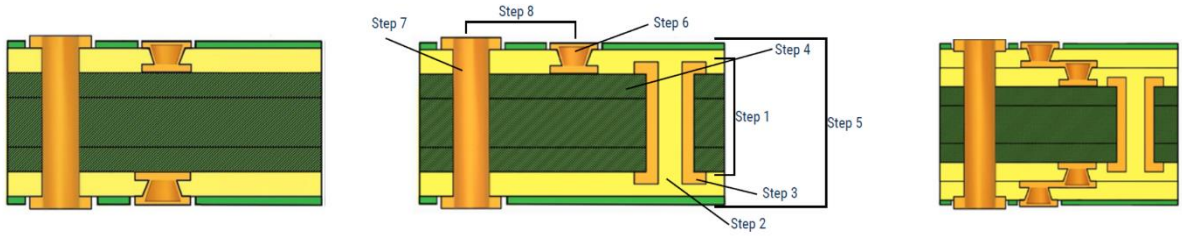

Figure 3 : HDI Stack-Up Types: 0-N-0, 1-N-1 and 2-N-2.

When designing your stack, think about the total number of lamination cycles, the quantity and span of mechanically and laser-drilled vias to minimise cost, maximise yield as well as reliability.

Once your artwork and stack design pass DFM, the layout can be tooled for manufacture and the fabrication of your PCB can begin. Traces and pads are produced by selectively removing copper and the build for a double-sided HDI board can be summarised by the following steps:

1. Multi-layer boards are built from the centre, staring with an inner base comprising an insulating dielectric clad with copper on both sides as shown below. Depending on the total number of layers, more of these cores are added,

insulated by a prepreg laminate which ‘glues’ the complete build during the bond press.

2. The artwork for each layer is printed using laser photo plotters: inner films are negative, *i.e.* the copper patterns left behind after processing are the clear areas. For the outer foils, the masks are positive and opaque traces and pads are the copper that remains. All the films are aligned by creating registration holes.
3. A light-sensitive photoresist is applied to the copper surfaces of each inner core, its mask placed on top and this assembly is then exposed to ultraviolet light as shown below. The clear areas of each film allow light to pass through, hardening the resist to create an image of the artwork. The exposed core is then washed using a chemical developer such as NaOH or Na_2CO_3 to remove any excess resist.
4. An etchant such as $FeCl_3$ or $Na_2S_2O_8$ is applied to each exposed inner layer to remove the copper not protected by the photoresist. Any excess resist is washed away leaving traces, pads and planes.
5. The inner layers are then optically inspected by comparing with the original artwork and registration holes are created to align all the cores.
6. The inner core panels are then chemically treated to improve the adhesion of the copper surface.
7. The stack is assembled comprising the inner core layers, each separated by a sheet of insulating prepreg. The build is aligned and bonded together under heat and pressure. The epoxy resin contained within the prepreg melts during the lamination process to bind and hold the stack.
8. The inner buried and blind via holes are drilled and plated to form an electrical connection between layers.
9. The top and bottom outer layers are exposed to their printed artworks, etched and tinned.
10. The outer layers are then optically inspected to ensure both copper surfaces are clean and any excess photoresist has been removed.
11. Both outer layers are aligned and assembled with the core of inner layers, separated by prepreg and the complete stack is re-bonded.
12. Through-hole and micro-vias drilled and plated.
13. Soldermask is applied to protect the top and bottom copper surfaces from environmental contamination such as oxidation and manual handling, and is also used to prevent the formation of shorting bridges during automated assembly by restricting where solder flows. Due to out-gassing concerns, not all space OEMs use it and some assembly sub-contractors have brewed their own cocktail of solder to control its flow.
14. Silkscreen is applied, however, due to out-gassing concerns, many space OEMs do not use it.
15. Surface finishes such as HASL, LF-HASL, OSP, ENIG, ENEPIG or hard gold are applied to cover and protect pads if required.
16. Electrical testing for shorts, opens, resistance, capacitance and continuity to ensure the PCB has been fabricated correctly. The measured results are

compared with the netlist to ensure the finished board matches the design intent. Typically, either a set of flying probes or a bed-of-nails are used to make contact with physical test points on the PCB.

17. Profiling to cut and remove your board from larger production panels.

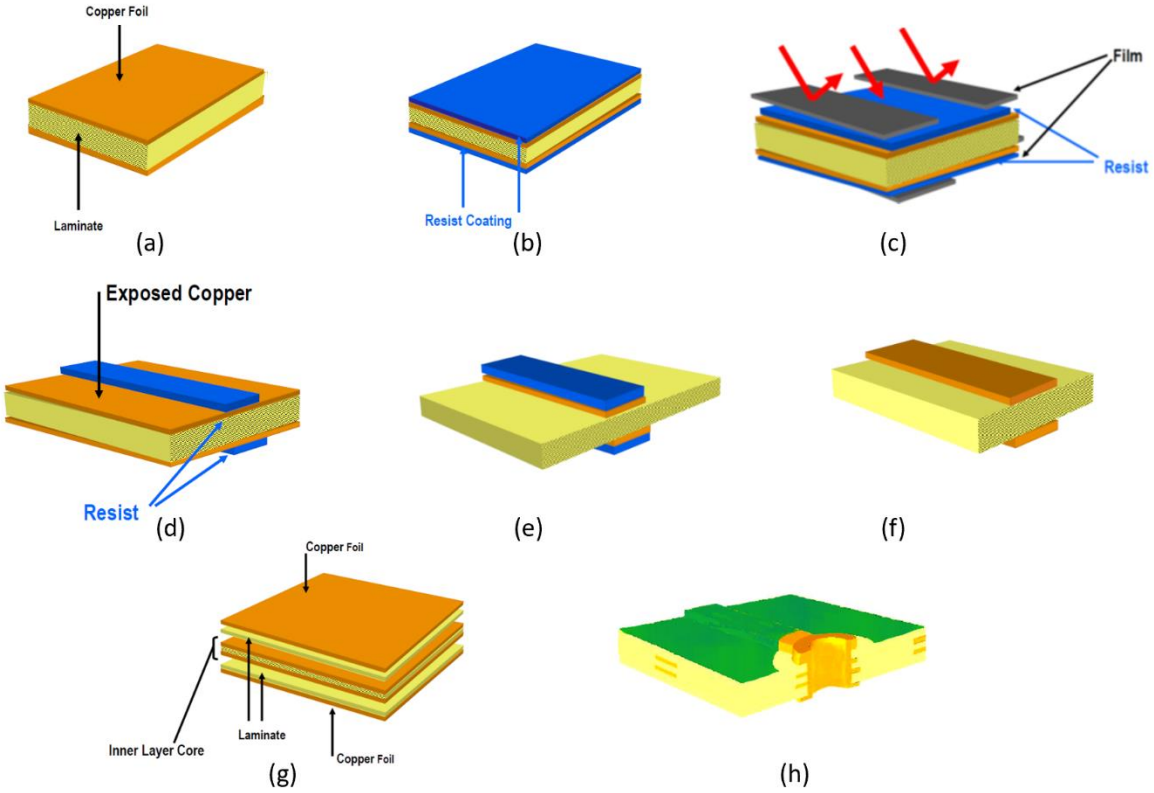

Figure 4 : (a) inner core (b) addition of photoresist (c) addition of artwork film and exposure to UV radiation (d) chemical developer removes resist from areas not polymerised by light (e) etch away copper not covered by resist (f) removal of resist (g) sequential lamination of outer layers (h) addition of soldermask.

There's a great video on YouTube that shows all the processes for a non-HDI board, *i.e.* a single press.

In addition to the trace width, conductor separation and clearance DFM checks listed above, you must become familiar with the above steps to create a PCB stack that minimises cost, maximises yield and crucially, ensures your board can be built and delivers the required performance right-first-time. Additional fabrication steps add more expense increasing the likelihood of loss!

The choice of material selection is important for HDI and space-grade PCB fabrication, *i.e.* will the dielectric meet the required electrical, performance, temperature and operational requirements? The thickness of the material affects impedance control and the aspect ratio of vias, while the allocation of the stack layers has a major impact on signal and power integrity, as well as EMC. Regardless of how all of the above are specified, fabrication is not an exact process as

lamination shrinks the dielectric and each vendor uses different equipment and methods resulting in build tolerances. Trace widths, separations and clearances are typically based on achieving a target characteristic impedance.

Most reputable fabricators manufacture bare-boards to IPC quality and reliability standards such as IPC-A-600J, IPC-601x, IPC-6012D and IPC-222x. The latter establishes generic guidelines for PCB design, component mounting and interconnections, with specific rules for rigid (2222), flex (2223), MCM-L (2225) and HDI (2226) boards. The IPC defines four quality classes which differ in the level of inspection based on the reliability and criticality of the final application, as well as the operating environment.

Class 1 – General Electronic Products

Class 2 – Dedicated Service Electronic Products

Class 3 – High Reliability / Harsh Operating Environment Products

Class 3/A – Space and Military Avionics

IPC Standard	Class I	Class II	Class III
Category	General Electronics	Dedicated Service Electronics	High-reliability Electronics
Life Cycle	Short	Long	Extended
Quality	Low	Good	Dependable
Product Examples	Toys	Laptops	Medical Devices

Table 1 : A summary of IPC's quality classes 1 to 3.

A manufactured PCB may have defects and the above standards define acceptable faults. Some will be purely cosmetic and will not impact the board's performance, while others can prevent reliable operation. Two useful IPC Manufacturing Coverage Standards Trees can be viewed here: 2221, 2222 and 7351 provide three producibility levels of features, tolerances, measurements, assembly and build verification.

In addition to the IPC documents, agencies such as ESA, NASA and ISRO have their own formal standards for space-grade boards. ESA's, ECSS-Q-ST-70-12C,

Design Rules for PCBs, and ECSS-Q-ST-70-60C, **Qualification and Procurement of PCBs**, are extensively used by the global space industry. The IPC also offers some interesting training courses on PCB design and DFM, and Spacechips teaches a course on **Right-First-Time, Space-Grade PCB Design, Layout, Manufacture & Assembly**.

Out-gassing is a concern for space-grade PCBs where gas trapped within the laminate, soldermask or silkscreen escapes during assembly or *in-orbit.* The former occurs when the board is exposed to high temperatures creating voids in the through-hole plating, while the latter has the potential to condense elsewhere and interfere with sensors. The fabrication process determines the quality of a board and off-gassing during soldering often occurs when the electroless copper plating is too thin (less than 20 µm) or the pre-heat process is done incorrectly. Choosing a dielectric material with a low out-gassing rate, tolerant to pressure and temperature variability, are key decisions to right-first-time PCB design for space applications. Providing a path for the gas to vent or baking boards in a vacuum can mitigate off-gassing by removing the residual moisture before actual use. NASA has developed a specific test procedure, SP-R-0022A, to evaluate materials for out-gassing.

Similarly, before sending your layout to the PCB fabricator, there are equivalent DFA checks to ensure that parts can be placed onto a shiny, new bare-board. Typical checks include verifying that the components match their pads, are adequately spaced from one another, edge-clearance rules are being applied, have the correct orientation, are positioned to allow visual or X-Ray inspection, the choice of package types to facilitate Pick & Place and/or automated soldering, and that parts are mounted with sufficient stress relief that they will not damage the PCB during vibration testing and thermal cycling. Size, pitch and separation tolerances are highly dependant on the equipment and processes used, and you must include your assembly sub-contractor early in the design cycle to ensure your populated PCB is delivered right-first-time, to cost and schedule. If there are parts close to the edge of the board, a border frame may be required by the Pick & Place machine. The total number of components and entries in the BoM impact the quantity of reel changes affecting cost and lead-time. Re-using standard package types and land patterns minimises risk!

The IPC quality classes previously introduced also apply to PCB assembly to grade the reliability of solder joints for through-hole components, surface-mount side and end overhang, minimum and maximum heel fillet height etc... Criteria for SMD passives and gulled-wing packages are illustrated below, and the maximum permittable value depends on whether the build is class 1, 2 or 3.

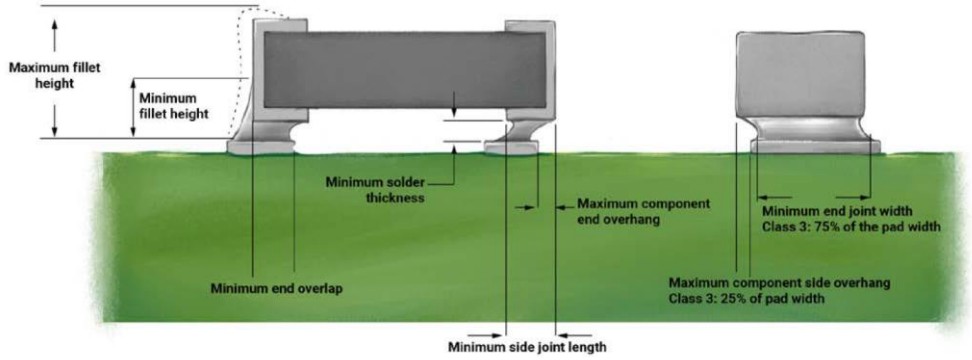

Figure 5 : DFA criteria for surface-mount passives.

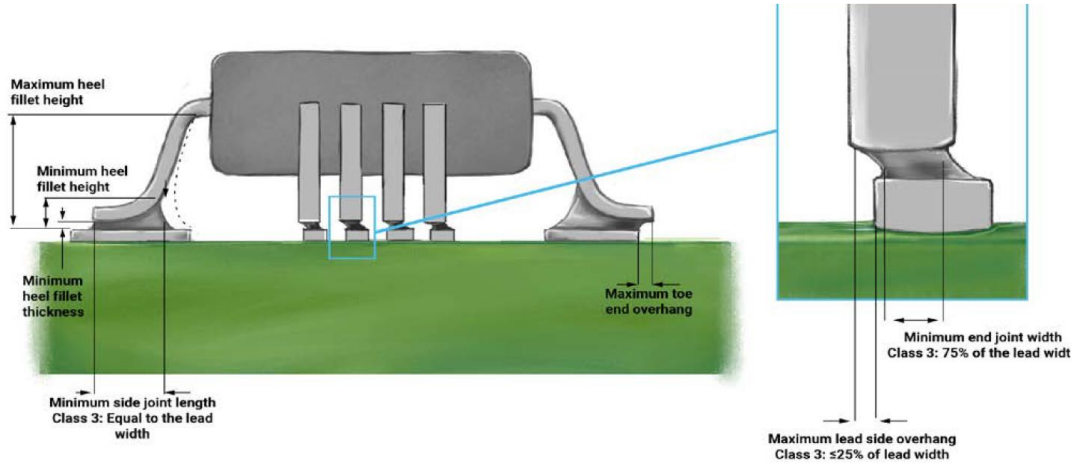

Figure 6 : DFA criteria for surface-mount, gulled-wing semiconductors.

Many space-grade OEMs apply a non-conductive, conformal coating to their assembled PCBs to protect against corrosion, moisture and airborne contaminants such as dirt and dust.

To meet your time-to-market needs, speak to your PCB fabricator and assembler before starting layout to understand their DFM and DFA rules respectively. At Spacechips, these are entered into Mentor's Constraints Manager to ensure the artwork is compliant as place & route progresses. Interactive DRC complains immediately if we violate these! By planning ahead, you can reduce the production lead-time, avoid re-designs, minimize fabrication and assembly costs, and guarantee a smooth transition from simulation to the EM and FM phases of product launch.

If you would like to learn more about DFM and DFA, I will be speaking at Siemens' User2User conference in Munich, Germany on May 12th. Until next month, the first person to tell me the difference between staggered and stacked micro-vias will win a Courses for Rocket Scientists World Tour tee-shirt. Congratulations to Marta from Austria, the first to answer the riddle from my previous post.

Dr. Rajan Bedi is the CEO and founder of Spacechips, which designs and builds a range of advanced, L to K-band, ultra high-throughput on-board processors, transponders and Edge-based OBCs for telecommunication, Earth-Observation, navigation, 5G, internet and M2M/IoT satellites. The company also offers Space-Electronics Design-Consultancy, Avionics Testing, Technical-Marketing, Business-Intelligence and Training Services. (www.spacechips.co.uk). Rajan can also be contacted on Twitter to discuss your space-electronics' needs: https://twitter.com/DrRajanBedi

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