RFSoC vs. Versal RF vs. Agilex Direct RF vs. AFE80xx vs. Elektra vs. AD9082 for Space Applications

Payload manufacturers are increasingly exploiting the SWaP advantages of single-chip, multi-channel transceivers, combining DSP and AI with RF ADCs and DACs. Devices offer significant benefits and flexibility to satellite operators allowing them to change receive and transmit frequency plans in-orbit to deliver better services and more insights.

Telecommunication operators can achieve better link performance, coverage and spectrum efficiency, while Earth-Observation users can transmit and receive multiple RF bands within the same orbital pass to monitor different terrains and penetration depths using a single transponder. SIGINT/ELINT operators can monitor UHF to K-band using one radio channel and the following example illustrates C and Ku-band carriers being simultaneously under-sampled at 3 GSPS with respect to their absolute centre frequencies, but over and bandpass sampled in relation to their information bandwidths:

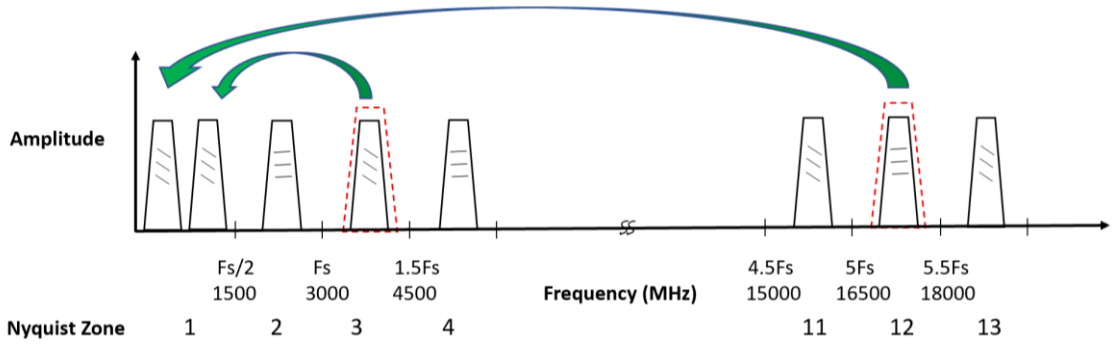


Figure 1 : Bandpass C and Ku-band carriers digitised at 3 GSPS [Spacechips].

Satellite applications are increasingly processing wider and re-configurable instantaneous bandwidths to deliver better services and more value-add. As a designer and manufacturer of software-defined transponders, Spacechips considers various single-chip transceivers for different customers. These enable operators to change receive and transmit frequency plans, information bandwidths, modulation and waveform types *in-orbit*, in response to varying communication and traffic needs. Integrated, multi-channel semiconductors such as RFSoC, Versal RF, Agilex Direct RF, AFE80xx, Elektra and the AD9082 offer obvious advantages such as smaller size, lower power consumption and in some cases, eliminating the external interfaces between the ADC/DAC and DSP. I remember doing the layout of the first Spacechips SDR1 prototype and the digital interface between the ADC and the FPGA required fifty impedance and length-matched traces as shown below:

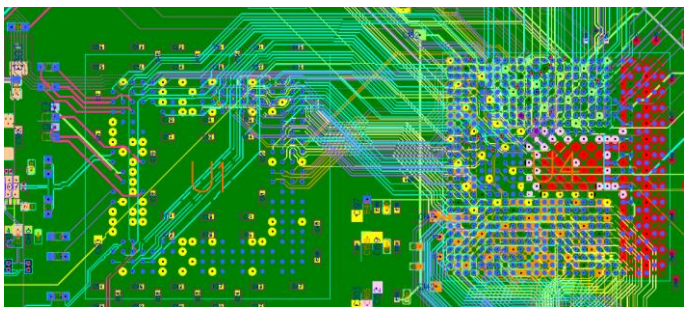


Figure 2 : ADC LVDS digital outputs (left) connected to FPGA (right) [Spacechips].

For almost two decades, transponder architectures have become more software-defined with traditional, analogue super-heterodyne circuits being replaced by digital and re-configurable logic. The latest, single-chip, multi-channel transceivers offer the potential to deliver true software-defined microwave and customers constantly ask: which microchip should they use, how can they improve ADC/DAC performance when directly processing RF carriers, will parts function reliably in space, do they have heritage, how can they implement in-orbit AI and machine learning, and how should they design-in the above parts. There's a big difference between evaluating these devices using dev. kits that accept a ±1V carrier and looking at its idealised output spectrum, to developing a payload baselining the same part, combining RF and high-speed digital, and delivering the advertised SNR and SFDR from a -120 dBm input! Does your test equipment have the sensitivity and RF bandwidth to prove this amplitude? There's also a huge disparity between powering a 10 W and a 120 W semiconductor!

Spacechips also teaches and demonstrates the RFSoC, Versal RF, Agilex Direct RF, AFE80xx, Elektra and AD9082 parts, and I've decided to share some insights and lessons learned. This first article will introduce and compare specifications, and discuss their suitability for satellite applications, while future posts will share design-in experiences and measurement results. Discrete, space-grade, broadband ADCs and DACs up to K-band are available, some of which offer advantages over the above devices, *e.g.* RF bandwidth, reliability, availability and qualified for use in space, and I have previously written about some of these.

I posted about AMD's RFSoC product family back in 2017 and Gen. 3 integrates a Zynq UltraScale+ MPSoC with 14-bit, 5 GSPS, 6 GHz ADCs and 14-bit, 10 GSPS, 6 GHz DACs. The DFE version operates up to 7.125 GHz and the original RFSoC was the first semiconductor to integrate high-speed mixed-signal convertors with an FPGA and ARM Cortex processors, removing the traditional physical interfaces between these technologies:

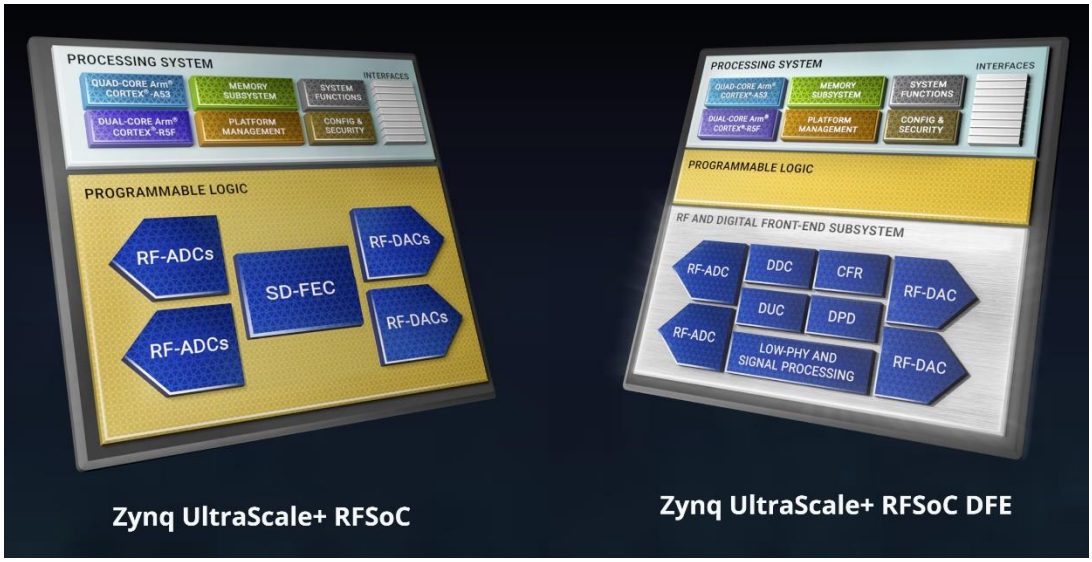
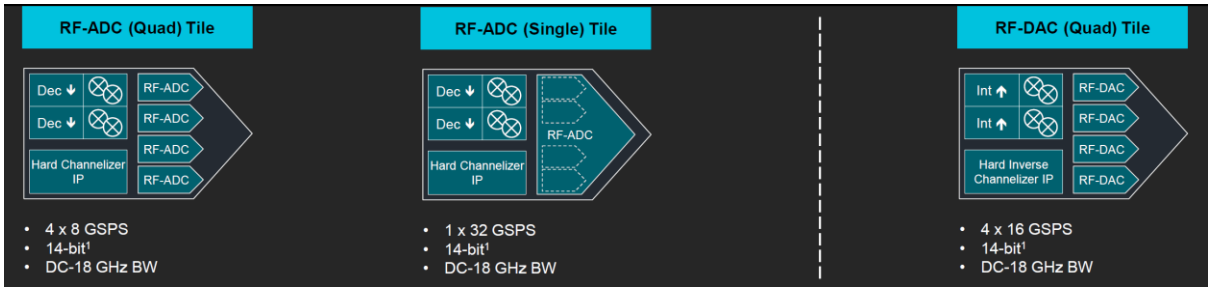


Figure 3 : Zynq UltraScale+ RFSoC [AMD].

AMD's Versal RF improves RFSoC by offering faster and wider bandwidth mixed-signal converters, *i.e.* 14-bit, 8/32 GSPS, 18 GHz ADCs and 14-bit, 16 GSPS, 18 GHz DACs. The Versal ACAP product range contains dedicated AI engines with vector processors to accelerate machine learning and AMD plans to formally qualify two devices from the new Versal RF product family: the VR1602 and VR1652 parts:



	Device Name			
	VR1602	VR1652	VR1902	VR1952
# 16 GSPS RF-DACs	**16**	**8**	16	16
# 8 GSPS RF-ADCs	**16**	**0**	16	0
# 32 GSPS RF-ADCs	**0**	**4**	0	8

Figure 4 : Versal RF Product Family [AMD].

Conceptually, Intel/Altera's Agilex 9 Direct RF family is similar to RFSoC, but offers faster and wider RF bandwidth mixed-signal converters enabling millimetre-wave sensing payloads, *i.e.* 10-bit, 64 GSPS, 36 GHz ADCs and 10-bit, 64 GSPS, 36 GHz DACs. Higher sampling frequencies enable digitisation and synthesis of wider instantaneous information bandwidths. A lower bandwidth, higher dynamic performance, sixteen channel, 14-bit, 4 GSPS, 7.1 GHz ADC and 14-bit, 12 GSPS, 7.1 GHz DAC version is also available. The Agilex 9 Direct RF FPGA contains significant tensor-capable DSP blocks within its fabric to support SIMD execution to accelerate AI operations.

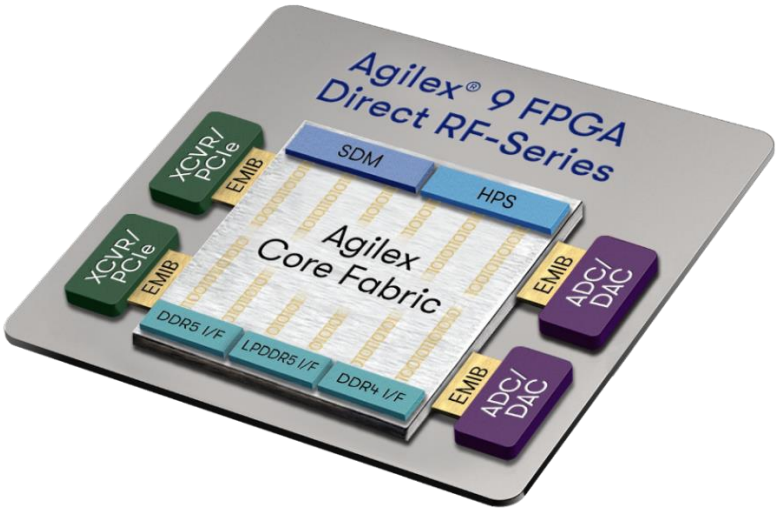


Figure 5 : Agilex 9 Direct RF [Altera].

Texas Instruments' AFE80xx is an integrated RF transceiver offering 14-bit, 4 GSPS, 7.1 GHz ADCs and 14-bit, 12 GSPS, 7.1 GHz DACs. The AFE80xx has eight JESD204B/C serial interfaces to connect to an ASIC or an FPGA at speeds up to 32.5 Gbps per lane. The AFE8010 part number is a ten-channel receiver only!

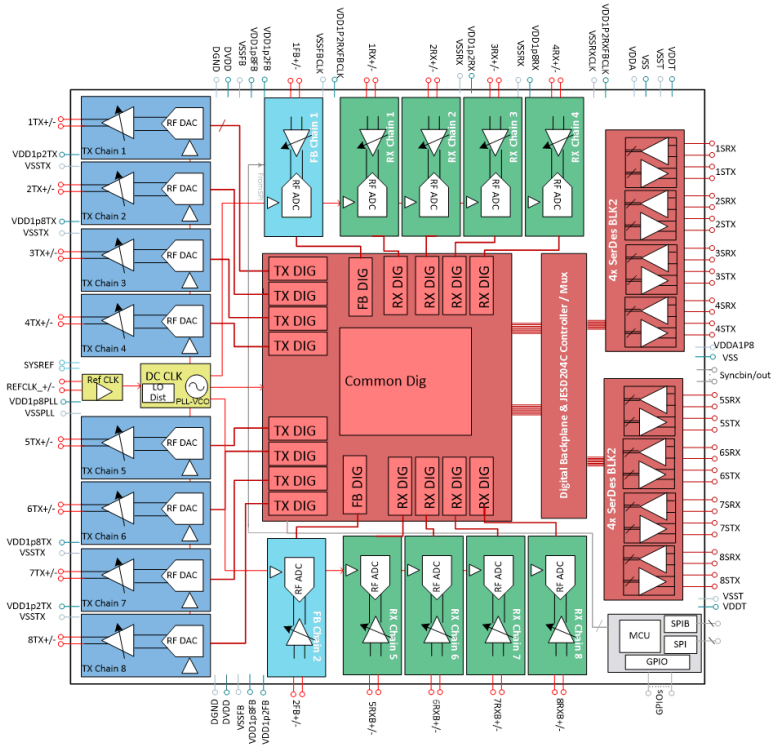


Figure 6 : AFE80xx Functional Block Diagram [Texas Instruments].

Jariet Technologies offers the Electra-MA/MK/MX dual-channel transceivers containing two 10-bit, 40 to 64 GSPS ADCs and DACs processing instantaneous bandwidths of 6.4 GHz up to 36 GHz. The Elektra devices have sixteen JESD204B/C interfaces to connect to an ASIC or an FPGA at speeds up to 30 Gbps per lane.

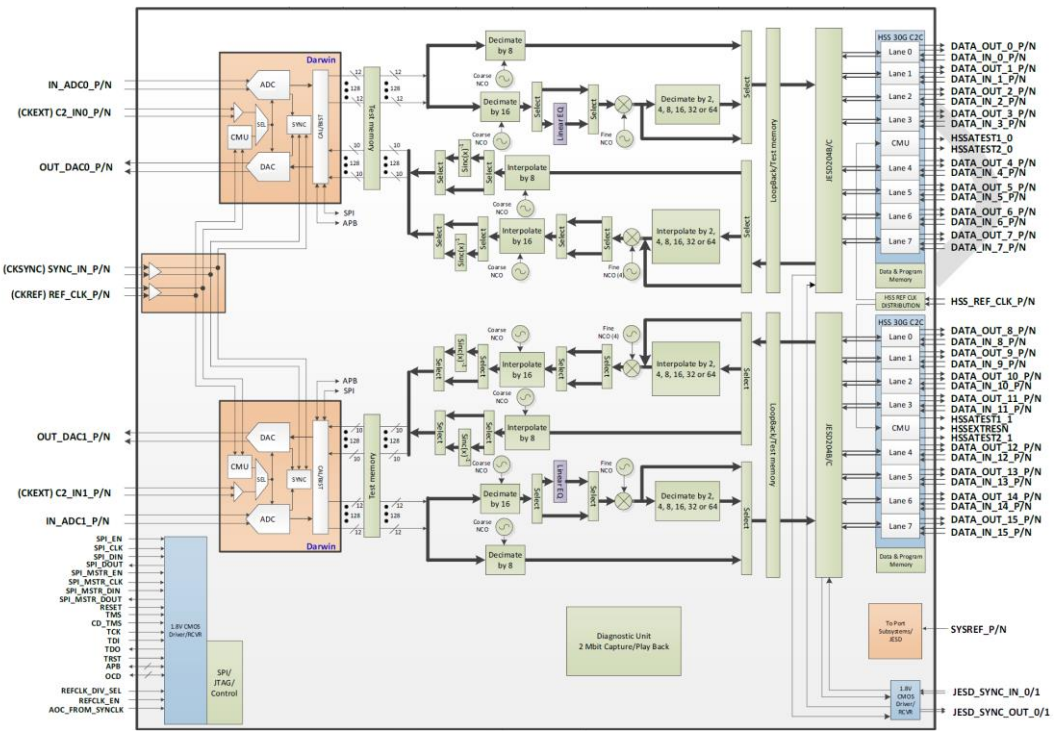


Figure 7 : Elektra Functional Block Diagram [Jariet Technologies].

Analog Devices' AD9082 integrates two, 12-bit, 6 GSPS, 8 GHz ADCs and four 16-bit, 12 GSPS, 8 GHz DACs. The AD9082 has sixteen JESD204B/C interfaces to connect to an ASIC or an FPGA at speeds up to 24.75 Gbps per lane.

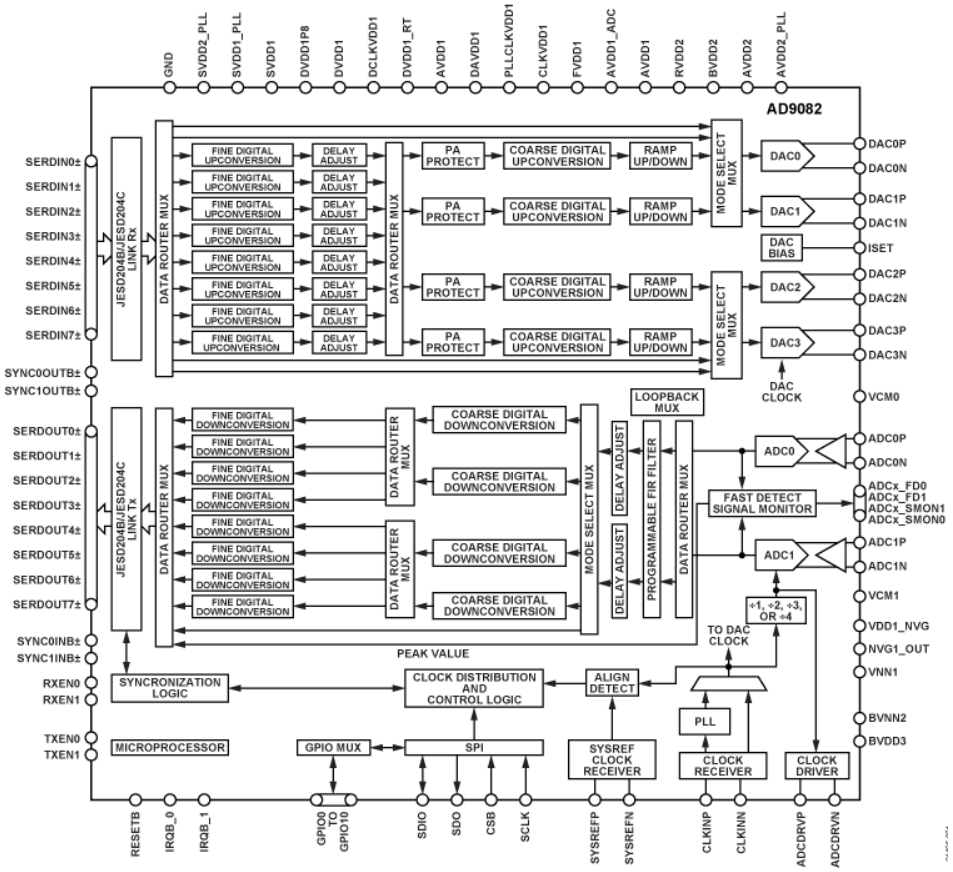


Figure 8 : AD9082 Functional Block Diagram [Analog Devices].

Spacechips has been asked many times, "***Which is the best device?***" Some of our clients need to perform a lot of real-time DSP and/or AI inference on the incoming carrier traffic, so a Versal RF or an Agilex 9 Direct RF is a better fit for their application. However, several of our customers do not and a large, complex, highly-integrated device requiring lots of power rails and watts is not their optimum solution. Two of our clients need more dynamic performance than that offered by ten-bit ADCs/DACs and exploiting the processing gain from over-sampling is one way to deliver higher SNR. Many users complain about not achieving the advertised data sheet performance and we teach how to extract every last dB of performance from these parts. Just because a device has a specified sampling/reconstruction clock frequency of ***Fs*** GSPS, this does not always result in an information bandwidth close to theoretical Nyquist, *i.e.* ***Fs/2*** Hz.

For some of our customers, there are financial and programmatic reasons that influence which part to baseline: one of our primes requires a year to approve a new supplier and this timeline did not fit with the project schedule and they developed an expensive, over-engineered system in my opinion.

For some of our clients, the physical size and/or power consumption of an integrated transceiver may be prohibitive, *e.g.* a 1U COTS payload might not have the area or financial budget, and its small platform may not be able to generate sufficient energy to supply a power-hungry device.

There are other integrated transceivers, but I focused on the ones that are of most interest to Spacechips and our customers. Most of the parts are part of a wider product family offering varying numbers of channels, resolutions and sampling speeds. The following table summarises the basic specifications of the six devices:

	RFSoC	Versal RF	Direct RF	AFE80xx	Elektra	AD9082
Architecture	FPGA,ARM, RX/TX ADC & DAC	FPGA,ARM, RX/TX ADC & DAC	FPGA,ARM, RX/TX ADC & DAC	RX/TX, ADC & DAC	RX/TX, ADC & DAC	RX/TX, ADC & DAC
Technology Node	16 nm FinFET	7 nm FinEFT	10 nm SuperFin	16 nm FinFET	12 nm CMOS	28 nm CMOS
Integrated FPGA	✓	✓	✓	×	×	×
ADC Resolution	14-bit	14-bit	10-bit	14-bit	10-bit	12-bit
Maximum ADC Sampling Rate	5 GSPS	32 GSPS	64 GSPS	4 GSPS	40 to 64 GSPS	6 GSPS
ADC RF Bandwidth	6 GHz	~18 GHz	36 GHz	7.1 GHz	6.4 GHz	8 GHz
DAC Resolution	14-bit	14-bit	10-bit		10-bit	16-bit
Maximum DAC Sampling Rate	10 GSPS	16 GSPS	64 GSPS	12 GSPS	40 to 64 GSPS	12 GSPS
DAC RF Bandwidth	6 GHz	~18 GHz	36 GHz	7.1 GHz	6.4 GHz	8 GHz
Maximum Instantaneous Bandwidth	~2 to 4 GHz	~16 GHz	> 20 GHz	0.4 to 1.2 GHz	6.4 GHz	~4 to 8 GHz
AI Acceleration	Fabric	AI Engines	Tensor Fabric	No	No	No

Table 1 : Comparison of Device Specifications.

All the parts contain integrated DDCs and DUCs to assist carrier digitisation and synthesis respectively, as well as re-programmability. For fixed frequency plans, bandpass carriers can be directly under-sampled and aliased into the baseband zone (see Figure 1). For example, for a 64 GSPS ADC, a 400 MHz-wide signal centred at 25 GHz can be digitised at 1 GSPS (bandwidth over-sampling of 2.5). For wider-band carriers, *e.g.* SIGINT spectrum monitoring or SATCOM gateways, you do not need to decide beforehand which signal you want, you can digitise the complete Nyquist bandwidth and using software DDC control, gain, filter and decimate the required signals. Some of the devices contain multiple independent DDCs to extract separate baseband streams. Decimation lowers the sample rate supplying the FPGA with data at 1 GSPS and not 64 GSPS in the above example, reducing memory bandwidth and easing FPGA resource utilisation. For CMOS devices, a lower switching speed also drops power consumption!

On the transmitting side, some of the DACs can directly up-convert baseband to IF/RF images in the higher Nyquist zones as illustrated below with an update rate of 10 GSPS. Similarly for wider-band carriers, a DUC can significantly reduce the data bandwidth to the FPGA, interpolate, up-convert, remove unwanted images and flatten the sinc roll-off within the desired passband. Changing frequency plans requires reprogramming the NCO rather than altering the analogue RF chain!

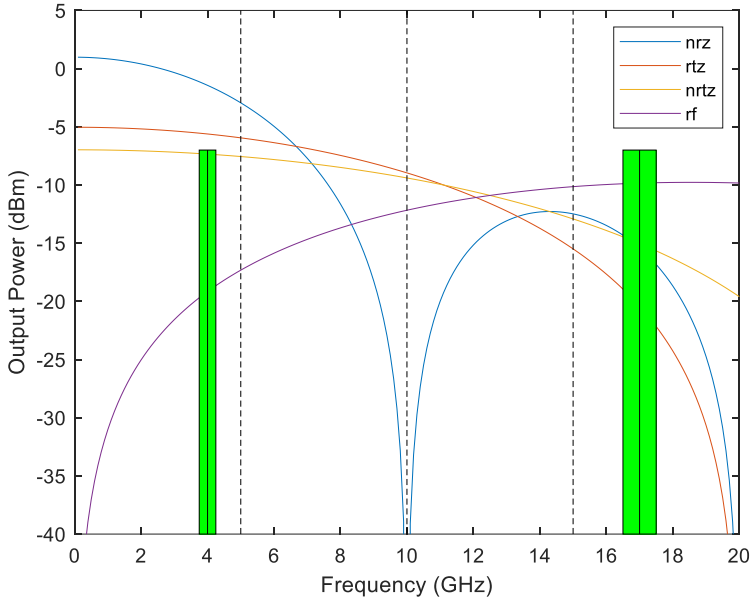


Figure 9 : C and Ku-band carriers in the first and fourth Nyquist zones [Spacechips].

None of the RFSoC, Versal RF, Agilex Direct RF, AFE80xx, Elektra the AD9082 parts were developed specifically for space applications, but several are currently operating in-orbit. All are fabricated using ultra-deep-submicron geometries, *e.g.* 16 or 7 nm FinFET, 10 nm SuperFin or 28 or 12 nm CMOS, and their thinner oxide as well as general scaling have made them intrinsically tolerant to total-dose changes over the lifetime of a mission. Several also contain process-level radiation-hardening to eliminate single-event latch-up. Device-level mitigation, *e.g.* the use of EDAC within fabric memory and triplicated HDL, as well as system techniques, *e.g.* power-rail monitors, have collectively improved overall reliability sufficiently for certain customers, resulting in very enabling transponder designs. Some of the devices have been irradiated and several are currently being tested in-beam.

My next article will describe using, testing and designing-in the RFSoC, Versal RF, Agilex Direct RF, AFE80xx, Elektra and AD9082 parts, all of which have unique requirements. Please note, the company and product names contained within this post are trademarked by their owners!

I'm off to the lab. to test several of the parts: until next month, the person who shares their best integrated transceiver design-in story will win a Spacechips' Training World Tour tee-shirt. Our global training schedule can be viewed at, The Global Space-Electronics Company, or contact, events@spacechipsllc.com, for more information.

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